Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A method of securing a multi-dimensionally constructed chip stack, the method which comprises:

providing a chip stack having a plurality of part chips connected to one another at respective contact areas, at least one of the part chips including functional components;

providing respective conductor tracks ~~in~~ within the part chips;

providing feed-through contacts at the respective contact areas for interconnecting the conductor tracks in the part chips such that that a continuous electrical signal path running through the part chips is formed;

transmitting an electrical signal from a transmitting device provided at a first end of the continuous electrical signal path to a receiving device provided at a second end of the continuous electrical signal path;

providing a continuous electrical reference signal path running from the transmitting device to the receiving device;

transmitting an electrical reference signal over the continuous electrical reference signal path at the same time as the electrical signal is transmitted; and

determining a damage to the chip stack by a determining device operatively connected to the receiving device when the electrical signal cannot be received, the determining device ensuring deactivation of security-relevant functional components in the part chips upon determination of damage in the chip stack.

Claim 2 (cancelled).

Claim 3 (original): The method according to claim 1, which comprises providing the transmitting device and the receiving device in different ones of the part chips.

Claim 4 (original): The method according to claim 1, which comprises providing a plurality of pairs of transmitting devices and receiving devices in different ones of the part chips.

Claim 5 (previously amended): In combination with a multi-dimensionally constructed chip stack including a plurality of part chips having respective contact areas, the part chips including functional components and being connected to one another at the respective contact areas, a device for securing the multi-dimensionally constructed chip stack, comprising:

conductor tracks provided within respective ones of the part chips;

feed-through contacts provided at the respective contact areas, said feed-through contacts interconnecting said conductor tracks of different ones of the part chips such that a continuous electrical signal path extending through the part chips is formed, said continuous electrical signal path having a first end and a second end;

a transmitting device provided at said first end of said continuous electrical signal path;

a receiving device provided at said second end of said continuous electrical signal path, said receiving device being configured to receive an electrical signal transmitted via said continuous electrical signal path;

a continuous electrical reference signal path extending from said transmitting device to said receiving device; and

a determining device operatively connected to said receiving device, said determining device determining that there is a damage to the multi-dimensionally constructed chip stack if the electrical signal cannot be received, said determining device ensuring deactivation of security-relevant functional components in the part chips upon determination of damage in the chip stack.

Claim 6 (original): The device according to claim 5, including a deactivation device operatively connected to at least one of the functional components, said deactivation device deactivating at least one of the functional components if said determining device determines that there is a damage to the multi-dimensionally constructed chip stack.

Claim 7 (original): The device according to claim 5, wherein said transmitting device and said receiving device are provided in different ones of the part chips.

Claim 8 (original): The device according to claim 5, including:

further transmitting devices and further receiving devices respectively provided in different ones of the part chips; and

said transmitting device and said receiving device forming a first pair of devices, said further transmitting devices and said further receiving devices forming further pairs of devices.

Claim 9 (original): The device according to claim 5, wherein said conductor tracks provided in the part chips are planar conductor tracks.

Claim 10 (original): The device according to claim 5, including:

a metallization layer formed between respective two of the part chips; and

further conductor tracks formed in said metallization layer for connecting the respective two of the part chips.

Claim 11 (original): The device according to claim 5, including a metallization layer provided on a side of an outer

one of the part chips, said metallization layer serving as a shield and having no connecting function.

Claim 12 (original): The device according to claim 5, wherein said continuous electrical signal path is a meandering path and runs vertically through the part chips.

Claim 13 (original): The device according to claim 5, wherein said conductor tracks are configured as planar, meandering conductor tracks in at least one of the part chips.

Claim 14 (original): The device according to claim 5, wherein the multi-dimensionally constructed chip stack has end faces and said conductor tracks are planar, meandering conductor tracks provided on the end faces.

Claim 15 (previously amended): A chip configuration, comprising:

a multi-dimensionally constructed chip stack including a plurality of part chips having respective contact areas, said part chips including functional components and being connected to one another at said respective contact areas;

a securing device for securing said multi-dimensionally constructed chip stack;

said securing device including conductor tracks provided within respective ones of said part chips, feed-through contacts provided at said respective contact areas, said feed-through contacts interconnecting said conductor tracks of different ones of said part chips such that a continuous electrical signal path extending through said part chips is formed, said continuous electrical signal path having a first end and a second end;

said securing device further including a transmitting device provided at said first end of said continuous electrical signal path, a receiving device provided at said second end of said continuous electrical signal path, said receiving device being configured to receive an electrical signal transmitted via said continuous electrical signal path, a continuous electrical reference signal path extending from said transmitting device to said receiving device, and a determining device operatively connected to said receiving device, said determining device determining that there is a damage to said multi-dimensionally constructed chip stack if the electrical signal cannot be received, said determining device ensuring deactivation of security-relevant functional

components in the part chips upon determination of damage in the chip stack.

Claim 16 (original): The chip configuration according to claim 15, including a deactivation device operatively connected to at least one of said functional components, said deactivation device deactivating at least one of said functional components if said determining device determines that there is a damage to said multi-dimensionally constructed chip stack.

Claim 17 (original): The chip configuration according to claim 15, wherein said transmitting device and said receiving device are provided in different ones of said part chips.

Claim 18 (original): The chip configuration according to claim 15, including:

further transmitting devices and further receiving devices respectively provided in different ones of said part chips; and

said transmitting device and said receiving device forming a first pair of devices, said further transmitting devices and said further receiving devices forming further pairs of devices.

Claim 19 (original): The chip configuration according to claim 15, wherein said conductor tracks provided in said part chips are planar conductor tracks.

Claim 20 (original): The chip configuration according to claim 15, including:

a metallization layer formed between respective two of said part chips; and

further conductor tracks formed in said metallization layer for connecting said respective two of said part chips.